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Application No.: 10/799391

Docket No.: CVZ-018

REMARKS

Claims 1-36 are pending of which claims 1, 4, 6, 20, 33 and 35 are independent. Claims 6, 9, 10, 15, 16, 20, 23-24, 27-29, 33 and 35-36 have been amended. No new claims have been added or deleted. No new matter has been added.

Claim Objections

Claim 36 was objected to as lacking a proper antecedent basis. Applicants have amended the claim and believe it now to be in condition for allowance.

Summary of Claim Amendments

Applicants have amended independent claims 6 and 20 to clarify that the schematic is a system-level schematic and amended the claims dependent thereon to correspond to the amended independent claims. Claim 33 was amended to correct an antecedent basis issue. Applicants have also made some minor form amendments to the medium claims.

Claim Rejections Pursuant to 35 U.S.C. §102(b)

Claims 1-13, 17-26 and 30-36 were rejected pursuant to 35 U.S.C. §102(b) as being anticipated by United States Patent Number 6,116,766 to Maseeh et al (hereafter "Maseeh"). Applicants respectfully traverse the rejection.

Argument

The claimed invention provides a process specification tool that is programmatically integrated with a system-level design and simulation environment thereby enabling the process-flexible design and simulation of Micro Electro-Mechanical Systems (MEMS) devices and other micro-fabricated devices. The process specification tool is a software tool for specifying the details of the fabrication process and enables the separation of the process specification data from the system-level design and simulation environment. The process specification tool retrieves the process data, which may include both a process specification and material

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properties. The separation of this process data from the system-level design and simulation environment allows the system-level model to have process-related parameters whose specification is not fixed, but rather is tied by reference to the process data. The tying of components to the process data allows the system-level environment to extract multiple process parameters for each component model instead of requiring duplicate entry of these parameters by the user in each component model, a time-consuming and error prone process. Modifications of the process data are programmatically communicated to the system-level environment. The dynamic response to changes in the process data allows alternative simulations to be run more effectively and quickly than in traditional IC design environments.

Each of the independent claims recite the claim limitation of a system-level schematic (claims 1, 6, 20 and 33) or a signal flow diagram (claims 4 and 35). Applicants respectfully suggest that the claim rejections incorrectly equate "system-level schematic" or "signal flow diagram" with "layout" (see Office Action paragraphs 4, 5 and 6, all citing col. 5, lines 12-14 as disclosing the limitation). The concepts of a system-level schematic and signal flow diagram on the one hand and a layout on the other are separate and distinct. The differences between the claim terms and the term "layout" are well understood as the terms are widely used in the electronics industry in general, and the electronics design automation (EDA) industry in particular.

A 'system level schematic' is a wiring diagram in which the wires represent electrical wires in the case of electrical circuits, or mechanical degrees of freedom in the case of a MEMS schematic. The symbols on the schematic are merely icons, that need not have any geometric significance, either in their shape and size, or in their relative placement on the 2-D plane on which the schematic is graphically represented (paper or a computer screen). Common electrical components such as capacitors, resistors and inductors have well-known symbols on schematics that bear no physical resemblance to their geometric implementation on an IC. In the case of a MEMS schematic, the symbols represent electro-mechanical entities, such as beams, rigid plates, flexible plates, electrostatic combs, electrodes, etc. A 'signal flow diagram' is an abbreviated diagram depicting signal flow in a system.

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In contrast, a 'layout', such as the one referred to in Maseeh, is a precise, to-scale, collection of geometric shapes such as polygons, circles, etc., that will be faithfully reproduced via photolithography techniques during IC fabrication. It is common practice throughout the electronics industry for engineers to design an electrical circuit by creating a schematic and then use EDA software to automatically generate the corresponding 2-D layouts. Thus the layout is separate and distinct entity from the system-level schematic or signal flow diagram. Maseeh discusses only a 2D layout and not the system level schematic or signal flow diagram claimed by Applicants.

Additionally, each of Applicant's independent claims recites a system-level design and simulation environment. The primary input to a system simulation is a schematic of some sort, as defined above and not a layout. A system simulator takes, at a minimum, a schematic as input, and numerically integrates a coupled system of ordinary differential equations (ODEs). The simulation result, or output, of the system simulator is a set of numerical values that represent the mechanical response (motion) of the MEMS to some physical stimulus. For signal flow diagram design and simulation, a signal flow diagram editor is used to specify model parameters for a signal flow diagram and a signal flow simulator is used to simulate the signal flow behavior of the device being modeled.

In contrast, the fabrication simulator described in Maseeh requires the precise 2-D geometrical description contained in the layout as input, and produces (via the Solid Modeler) a 3-D solid model. The concept of a solid model is well understood in the mechanical computer-aided design (CAD) industry. A solid model is a stationary 3-D geometrical shape that, in this case, may represent a MEMS. In order to predict the mechanical response of the MEMS, Maseeh includes the further steps of discretizing the solid model into finite elements and then performing boundary-element analysis and/or finite-element analysis rather than the claimed system-level simulation. Both boundary-element analysis and finite-element analysis entail solving a coupled system of partial differential equations (PDEs), which involves different algorithms and methods, and generally requires a lot more computing time, than solving coupled ODEs. In comparison, the claimed system-level simulation directly results in a prediction of mechanical response without performing "fabrication simulation", i.e.: creating a 3-D solid model and performing the further steps of discretizing the model into finite elements and then

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performing boundary-element or finite-element analysis. Accordingly, Maseeh can not be said to disclose the claimed simulation environment.

Since Maseeh discloses neither the claimed simulation environment or the system level schematic or signal flow diagram specified by Applicants' independent claims, Applicants respectfully suggest all of the pending claims 1-35 are in condition for allowance.

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CONCLUSION

In view of the above, Applicants believe the pending application is in condition for allowance.

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